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A New Structure for Cascaded Single-Stage Distributed Amplifier Using Proposed Active Inductor Loads

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Abstract:

A modification to cascaded single-stage distributed amplifier (CSSDA) design by using active inductor is proposed. This modification is shown to render the amplifier suitable for high gain operation in small on-chip area. Microwave office program simulation of the Novel design approach shows that it has performance compatible with the conventional distributed amplifiers but with smaller area. The CSSDA is suitable for optical and satellite communication systems.

Keyword: Micro electronic, Microwave, Amplifier, Distributed Amplifier.

1 Introduction:

The conventional distributed amplifier (CDA) was proposed in 1948 and originally applied to vacuum tubes [1]. With the development of monolithic microwave integrated circuits (MMIC) during 1960's [2], the DAs have been realized by using on-chip transistor technologies such as MOSFET's [3], and MESFET's [4], as well as GaAs MESFET [5]. More recently many other technologies were introduced to the monolithic distributed amplifier world[6]. A schematic representation of a DA is shown in Figure(1). In this structure, the parasitic capacitors of the transistors (Cgs and Cds) together with the inductors (Lg and Ld) make two artificial transmission lines (gate and drain lines). As a result, the effect of these capacitors will be absorbed into Low-pass filter segments of the transmission lines then it is possible to obtain amplification over much wider bandwidth. The drawback of this amplifier is limited gain-bandwidth due to its optimum number of stages [7]. High gain can be achieved by cascading several single stage distributed amplifiers. The circuit structure of CSSDA is shown in Figure (2). It is essentially a cascade connection of single–stage distributed amplifiers with the omission of idle gate and drain termination for the intermediate stages [8]. The amplifier's gate transmission line is formed by the lumped inductors L_I and the gate capacitance Cgs of T_1 where as the inductors Ld along with the drain capacitance Cds of T_N serve as the drain artificial line. These input and output lumped transmission lines match the amplifier to the source and load impedance R_o over the entire bandwidth. The available power gain expression is given by [9]:

$$G = \frac{g_m^{2N} R_I^{2(N-1)} R_o^2}{4} \qquad \text{.....(1)}$$

Where g_m is the transconductance of the active devices. The input and output artificial lines possess much larger bandwidth compared with that of the inter-stage loads, therefore the bandwidth of the amplifier is limited by the cutoff frequency of internal stage (T_2 -T_{N-1}).

It is given by:

$$w_c = w_{ci}\sqrt{2^{(\frac{1}{N-1}-1)} + \frac{1}{m} - \frac{1}{2m^2} + \sqrt{2^{(\frac{2}{N-1}-2)} + 2^{(\frac{1}{N-1})}\frac{1}{m} + 2^{(\frac{1}{N-1}-1)}\frac{1}{m^2} + \frac{1}{4m^4} - \frac{1}{m^3}}}$$

…….(2)

Where $m = L_I / R_I^2 C$, $C = Cgs + Cds$, and $w_{ci} = 1/R_I C$ is the cutoff frequency of the stages if there is no inductance in the drain line of the amplifier. Equation (2) can be written as follow:

$$w_c = w_{ci} \cdot \gamma \qquad \text{…….(3)}$$

Table (1) lists some values of *m* and their corresponding to various values of γ for N=4.

Table.1

m	γ	Response
0	1	No inductive load
0.9	1.53	Maximum bandwidth
0.5	1.34	Maximally flat

Referring to equation (1), it is clear that high gain is obtained with large R_I. Since $L_I = mR_I^2 C$, large R_I mandates large L_I for given m and C where by the size of the on-chip circuit will be increased. The goal of this paper is to study this problem and to put a suggestion for an effective size reduction for the on-chip circuit.

2 Implementation of On-chip Inductor:

The main problem associated with the design of microwave integrated circuits, such as amplifiers, oscillators and mixers in which the inductors are essential elements is the physical size of these elements. Both resistors and capacitors are easy to implement. Considerable effort has gone into the design of the inductor implementation. Figure(3) shows the layout for different types of spiral inductors. For a given shape, an inductor is completely specified by the number of turns (n), the turn width (w), the turn spacing (s), and the turn diameters: d_{in} and d_{out} , where $d_{avg} = 0.5(d_{in} + d_{out})$. There are many expressions for the inductance value, one of them is given by a monomial expression that has the following form

[10] $$L = b d_{out}^{a_1} w^{a_2} d_{avg}^{a_3} n^{a_4} s^{a_5}$$

…….(4)

Where the coefficients β and α_i are layout dependent. For a square, $\beta = 1.62 * 10^{-3}$, $\alpha_1 = 1.21$, $\alpha_2 = -0.147$ $\alpha_3 = 2.4$, $\alpha_4 = 1.78$, and $\alpha_5 = -0.03$. It is clear that the value of L depends on the size of its layout.

3 Proposed Active Inductor Implementation:

Figure (4-a) shows a single stage distributed amplifier. The introduction of a current source transistor M_L in the load circuit alters its frequency dependent impedance, Figure (4-b).

$$Z_L = \frac{V_x}{i_x} = R + \frac{1 + g_m R}{1 - w^2 C g_s L}(jwL)$$

$$Z_L \approx R + jw(g_m RL) \qquad \text{…….(5)}$$

$$Z_L = R + jwL_{act}$$

where $L_{act} = g_m RL$ …….(6)

Equation (6) shows that the amount of amplification achieved in the inductance value is (g_mR) which means that the effective inductance is (g_mR) greater than the actually implemented one. This allows the use of a large value inductance in the circuit but with a small on-chip area. Although the new structure of the inductance composed of two elements instead of one, the transistor has a very small area compared with the area of the inductor.

4 CSSDA with Active Inductor Loads:

Previous CSSDA's have used large inductances at the drains. Increasing

the gain of the amplifier is achieved either by increasing the value of R_I in equation (1), or by increasing the number of stages (N). Since m = L_I/R_I^2C, then large R_I mandates large L_I for a given m and C. On the other hand increasing N with a given value of L_I means increasing the size of the amplifier. These two points yield circuits with larger on-chip area. However, Figure (5) shows the schematic of a CSSDA designed with a new type of inductors called "Active Inductors" , each one composed of an active device (M_i) plus a small inductor. Such implementation of inductors reduces the overall on-chip circuit area without any effect on the performance of the amplifier. The available power gain can also be determined using equation (1). A RF signal from a matched generator is coupled by the transconductance of the active device (T_i) at each stage, and finally terminated by the matched output load port. At each stage, the RF signal will be boosted and terminated by the load resistor (R_I). The amplified signal is valid only up to the cut-off frequency, which is controlled by the elements values of equation (2). To demonstrate the effectiveness of the developed methodology, a four stage amplifier is designed with gain about 23dB and bandwidth of 10 GHz. The elements values are: R_I = 40 Ω , L_I = 0.42 nH , C = 0.6 pf , and g_m = $0.06\,\Omega^{-1}$. The circuit was implemented using microwave office program. The S-parameters extracted from the measurement data are shown in Figure (6). The circuit is also implemented using active inductors (with L_I = 0.1 nH and g_m = $0.15\,\Omega^{-1}$) and its measurement data are shown in Figure (7). It is interesting to note that, compared to the conventional CSSDA, the CSSDA with active inductor loads achieve the same results (forward gain S_{21} the reflection losses S_{11} and S_{22}) but with smaller inductance.

5 Conclusion:

In this paper a new design of cascaded single-stage distributed amplifier using the novel active inductor loads is demonstrated. The new structure has unique benefits over the conventional CSSDA in terms of high gain and area saving. The structure also allows very simple design procedure. A four-stage amplifier was implemented using the developed technique to achieve gain ≈23 dB and bandwidth ≈ 10 GHz. Hence, the CSSDA design is suitable for optical and satellite applications.

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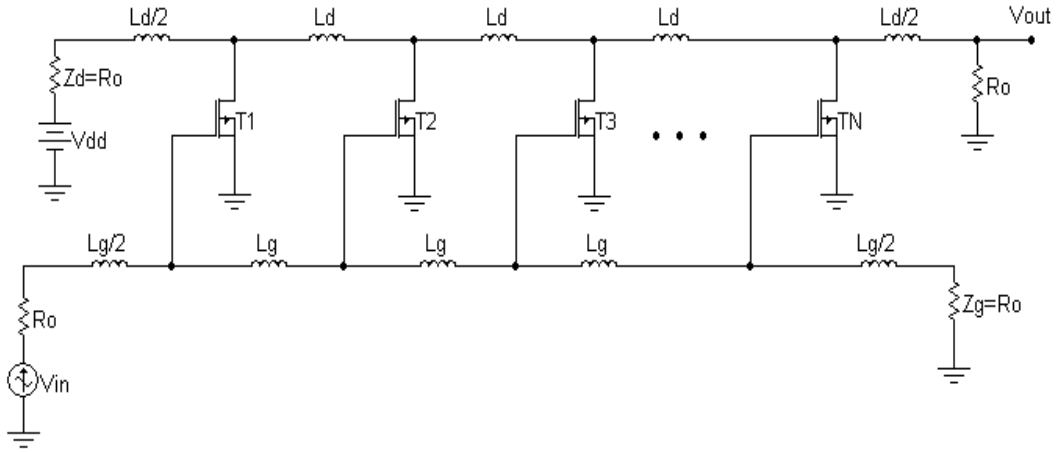
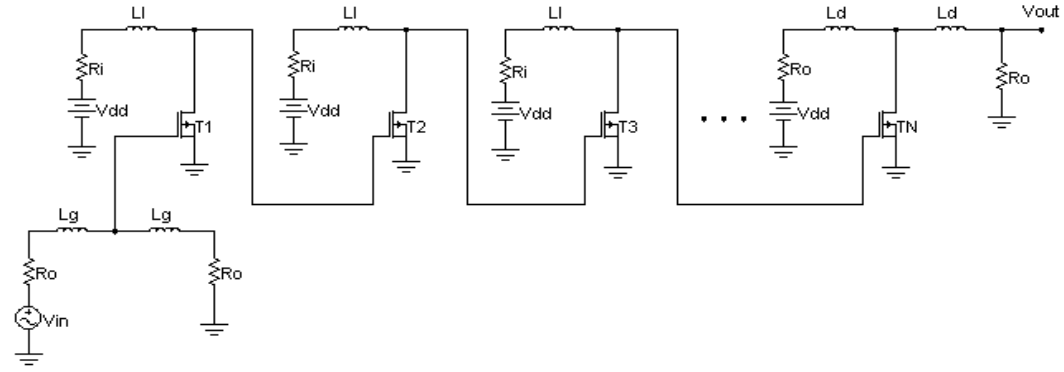
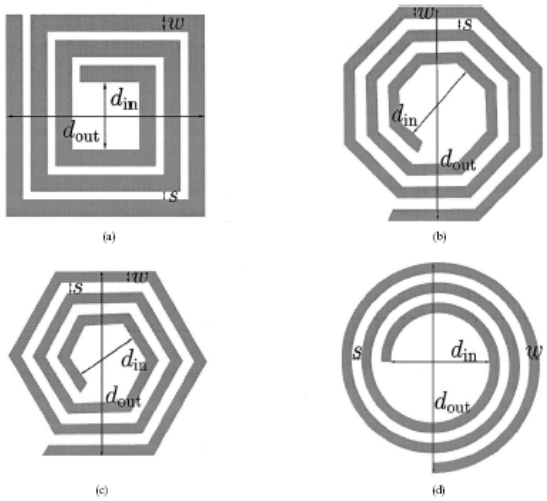


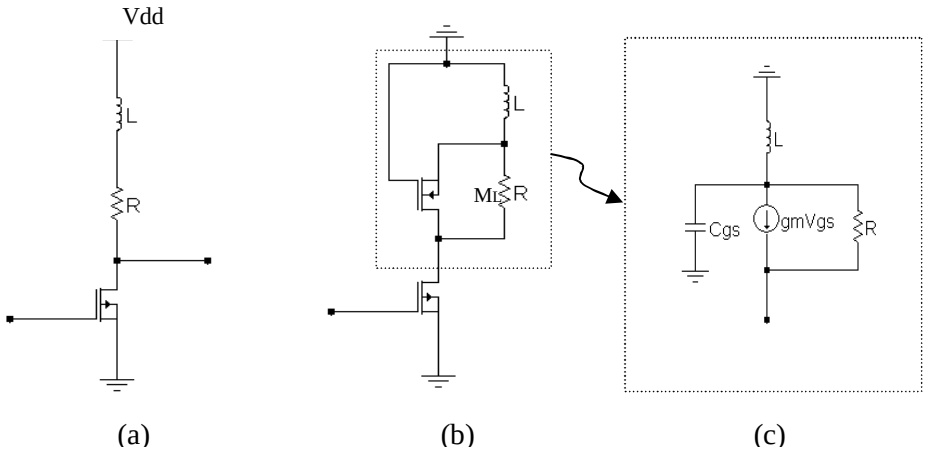
Figure(1) Schematic circuit of N-stages CDA



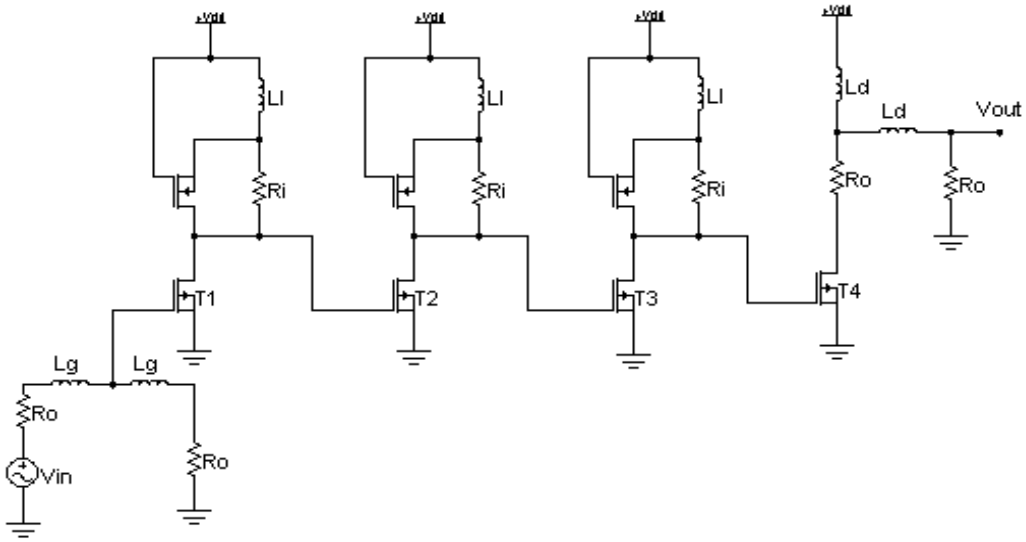
Figure(2) Schematic circuit of N-stages CSSDA



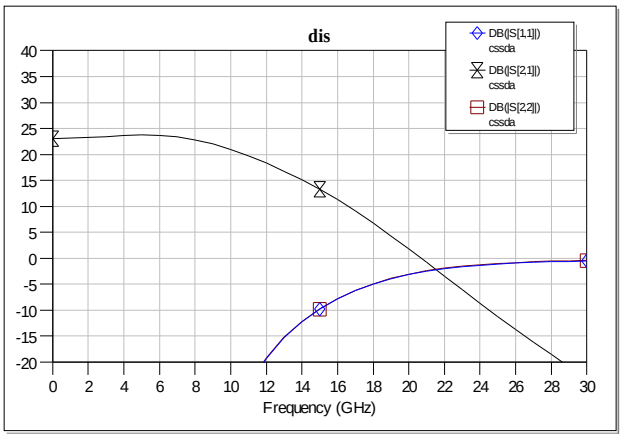
Figure(3) On-chip spiral inductor realizations: (a) square, (b) hexagonal, (c) octagonal, and (d) circular.



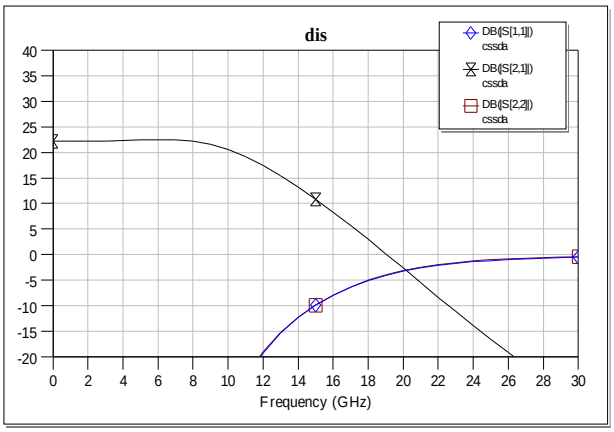
Figure(4) Single stage of DA.(a)simple common source amplifier.(b)the amplifier with active inductor.(c)the equivalent model of the active inductor.



Figure(5) Proposed CSSDA



Figure(6) Simulated S-parameters in the CSSDA with passive inductors (L_I= 0.42 nH)



Figure(7) Simulated S-parameters in the CSSDA with active inductors (L_I= 0.1 nH)

هيكلة جديدة للمضخمات التوزيعية باستخدام احمال حثية فعالة

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الخلاصة:

البحث يتناول دراسة موجزة لمضخمات أشارات الترددات المايكوية ذات النطاق الواسع جدا باستخدام مبدا (Cascaded Single Stage Distributed Amplification) الذي يستخدم بشكل كبير في تطبيقات الاتصالات البصرية و انظمة الاتصالات عبر الاقمار الصناعية. هذا النوع من المضخمات يضم في تركيبته محاثات في دائرة الخرج. ان حجم المحاثة هو احد اهم المشاكل التي ترافق تصميم الدوائر المتكاملة (integrated circuits) للانظمة المايكروية, لذلك تم تطويرهذه التقنية من المضخمات بحيث اصبحت تستخدم نوع مستحدث من المحاثات سميت "محاثات فعالة" الهدف الاساسي منها هو انها تحتاج مساحة اقل عندما تصمم على الدوائر المتكاملة .التشكيل الجديد للمضخم أختبر باستخدام برنامج (Microwave Office) الذي هو مختص بالانظمة المايكروية وكانت نتائج الاختبار هو ان المضخم الجديد مطابق بكفائته للمضخم التقليدي مع فرق انه يحتاج حجوم اصغر للمحاثات .