



Design & Implementation of High Switching & Low Phase Noise Frequency Synthesizer

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Abstract:-

This research describes the design & implementation of frequency synthesizer using single loop Phase lock loop with the following specifications: Frequency range (1.5 – 2.75) GHz, Step size (1 MHz), Switching time 36.4 μ s, & phase noise @10 kHz = -92dBc & spurious -100 dBc

The development in I.C. technology provide the simplicity in the design of frequency synthesizer because it implements the phase frequency detector (PFD), prescaler & reference divider in single chip. Therefore our system consists of a single chip contains (low phase noise PFD, charge pump, prescaler & reference divider), voltage controlled oscillator, loop filter & reference oscillator. The single chip is used to provide the following properties:

- Low power consumption.
- Small size, light weight.
- Flexibility in selecting crystal oscillator frequencies to fit into the system frequency planning.
- High reliability.

The application of this synthesizer in frequency hopping systems, satellite communications & radar because it has high switching speed, low phase noise & low spurious level.

1. Introduction

The generation of accurate waveforms plays a crucial role in almost all electronic equipment, from radar to home entertainment equipment. A frequency synthesizer is defined as a system that generates one or many frequencies derived from a single time

base (frequency reference), in such a way that the ratio of the output to the reference frequency is a rational fraction. The frequency synthesizer output frequency preserves the long-term frequency stability (the accuracy) of the reference and operates as a device whose function is to generate frequencies that

are multiples of the reference frequency (multiples by a single or many numbers). These multiples may be whole or fractions; but since only linear operations are used (in the frequency domain), these numbers can only be rational. A frequency synthesizer, as defined here, can thus generate an output frequency of, say, X/Y (where X and Y are whole numbers) times the reference frequency.

PLL synthesizers can be found in the most sophisticated radar systems or the most demanding satellite communications terminals as well as in car radios and stereo systems for home entertainment. The PLL is a feedback mechanism locking its output frequency to a reference. PLL synthesizers gained popularity for their simplicity and economics.

Frequency synthesizers use a PLL to copy, multiply, or divide a crystal reference source. The stability and phase noise properties of the crystal reference oscillator are preserved within the loop bandwidth of the PLL[2].

2.Frequency Synthesizer Requirements

The basic requirement set for a frequency synthesizer by any telecommunications system is that the synthesizer must be able to generate all required frequencies with a sufficient accuracy. The output signal of an ideal frequency synthesizer is a pure sinusoid, i.e. a delta function in the frequency domain. The output spectrum of a real synthesizer, however, consists of a number of nonideal components in

addition to the sinusoidal component. Figure 2.1 illustrates these components, as well as other parameters, whose specifications will be derived in the following sections.

2.1.Phase Noise It is divided into two types:-

2.1.1Phase noise at small offset frequencies

In the transmitter, the major contributor to the phase error is the frequency synthesizer generating the local oscillator frequency. The close-in phase noise manifests itself as random fluctuations in the phase of the local oscillator signal, which then translate directly to fluctuations in the phase of the transmitted signal, i.e. random phase error. Let us assume that the frequency synthesizer is a second-order PLL, i.e. the phase noise rolloff is -40 dB per decade for offset frequencies beyond the loop bandwidth. Let us also assume that the phase noise floor of the synthesizer is low enough to be ignored as a contributor to the total integrated noise. This assumption is only valid for narrow band systems, where the PLL bandwidth is only about an order of magnitude smaller than the channel bandwidth. Let us denote the phase noise at small offset frequencies by $L_{close-in}$, the phase-locked loop bandwidth by B_{PLL} , and the channel bandwidth of the system in question by $B_{channel}$. We can now approximate the square of the phase error with[3].

$$\phi_e^2 \approx \int_{-B_{channel}/2}^{-B_{PLL}} L_{close-in} \left(\frac{-B_{PLL}}{f} \right)^4 df + \int_{-B_{PLL}}^{B_{PLL}} L_{close-in} df + \int_{B_{PLL}}^{B_{channel}/2} L_{close-in} \left(\frac{B_{PLL}}{f} \right)^4 df.$$

Eq(2.1)

Solving for the close-in phase noise, we get:

$$L_{close-in} \leq \frac{3}{8} \frac{\phi_e^2 B_{channel}^3}{B_{PLL} (B_{channel}^3 - 2B_{PLL}^3)} \quad \text{Eq (2.2)}$$

shows that increasing the PLL bandwidth leads to a tighter specification for the close-in phase noise.

2.1.2. Phase noise at large offset frequencies

The phase noise of the frequency synthesizer at large offset frequencies is almost always specified. The reason for this is a phenomenon commonly referred to as *reciprocal mixing*. The phase noise tail of the local oscillator signal mixes with undesired interfering signals, and the mixing result ends up at the same intermediate frequency as the wanted signal, thus impairing the signal-to-noise ratio. The reciprocal mixing phenomenon is illustrated in Figure 2.2. The spectrum converted to the intermediate frequency can be represented as the convolution of the received RF spectrum and the spectrum of the local oscillator signal (Equation (2.3)).

$$S_{IF}(\omega) = S_{RF}(\omega) \otimes S_{LO}(\omega) \quad \text{Eq(2.3)}$$

Since the interfering component can be much stronger than the wanted signal, the phase noise power of the local

oscillator at the same offset frequency must correspondingly be much lower to maintain a useful signal-to-noise ratio of the down converted signal. The specification for the local oscillator power at a given offset frequency can be derived from the power levels of the wanted signal and the interfering signal, and the signal-to-noise ratio required to guarantee signal reception at the desired bit error rate:

$$L(\Delta f) \leq P_{wanted} - P_{unwanted} - SNR_{required} - 10 \cdot \log(B_{channel}) \quad \text{Eq(2.4)}$$

The last term of the equation is an approximation, assuming that the mean value of the phase noise over the channel bandwidth can be approximated with the phase noise value at the center point of the channel.

2.2. Spurious tones

Spurious tones are unwanted components in the frequency synthesizer output spectrum that are not noise-like. The VCO is essentially a frequency modulator, and periodic signals at the VCO control line will result in an output signal with discrete FM sidebands. The requirement for the maximum spurious power derives from the blocking specification of the telecommunications

system. A spurious tone at a given offset mixes the neighboring channel at the same offset down to on top of the wanted channel. The spurious power must therefore be low enough to provide an adequate signal-to-noise ratio (SNR) in the output of the receiver. A number of nonidealities in the PLL itself will generate interfering signals in the VCO control line. All of these phenomena will result in periodic signals at the PLL reference frequency, and thus in spurs at an offset of f_{ref} from the carrier. The dominant spurious-generating nonidealities in a typical PLL are mismatch between the up and down currents in the chargepump and charge injection through the switches in the chargepump. Also, the leakage currents of the chargepump and the VCO may be significant contributors.

Figure 2.3 shows how the mismatch between the up and down currents in the chargepump results in a periodic signal in the VCO control line. In this case, the up current is slightly larger than the down current. The PLL feedback mechanism tries to keep the mean value of the VCO control voltage (V_C) constant, and therefore the down pulses from the phase detector will be slightly longer to compensate for the smaller current. The resulting net output current of the chargepump (I_{CP}) is then low pass filtered in the loop filter. Despite of the filtering, the VCO control voltage still clearly shows a periodic beat at the reference frequency, which will in turn result in spurious tones[4]. The charge injection through the chargepump switches is illustrated in Figure 2.4. The digital up and down signals from the phase detector will have relatively fast rise and fall times, and thus harmonic components at very high frequencies.

Some of these high-frequency components will be injected to the chargepump output node through the gate-source and gate-drain capacitances (C_{GS} and C_{GD}) of the switch transistor. The capacitances C_{GS} and C_{GD} depend on the gate-to-source and gate-to-drain voltages V_{GS} and V_{GD} , respectively. Therefore, the charges injected through the up and down switches will depend on the chargepump output voltage. The up and down charges will be equal for one single output voltage value. For all other output voltages, there will be a net charge injected to the output of the chargepump. The PLL will compensate for this excess charge very much in the same way as the chargepump mismatch in Figure 2.3, and a periodic beat at the reference frequency is generated.

The other phenomenon typically generating reference spurs is the loop filter leakage. When the PLL is locked, the chargepump is neither pumping up nor down for most of the time. Ideally, a chargepump in this state represents an infinite impedance towards the loop filter. Likewise, the input impedance of the VCO control node is ideally infinite. In practice, however, both the chargepump switches and the VCO control node (typically connected to a varactor diode) will have finite impedances, and there will be a small leakage current that will change the control voltage of the VCO slightly either up or down. The PLL will compensate for the leakage, and thus a periodic beat at the reference frequency is again generated. In PLL's using a discrete loop filter, the leakage currents are normally not a problem. The loop filter capacitors are very large, and a small leakage current will change the loop filter voltage only negligibly. Since

the spurious power will depend on the actual shape of the interfering waveform. It is first assumed that the disturbance on the VCO control line appears as narrow, rectangular pulses having a width Δt and

a height ΔV . Inserting the Fourier series expansion of the rectangular waveform into the time domain representation of the VCO output waveform yields the following equation for the VCO output:

$$v_{out}(t) = V_0 \cos \left[\left(\omega_0 + K_{VCO} \frac{\Delta V \Delta t}{T_{ref}} + K_{VCO} V_{CTRL} \right) t \right] - K_{VCO} \left[V_{CTRL} \sum_{n=0}^{\infty} \frac{a_n}{n \omega_{ref}} \sin(n \omega_{ref} t + \theta_n) \right] \sin \left[\left(\omega_0 + K_{VCO} \frac{\Delta V \Delta t}{T_{ref}} + K_{VCO} V_{CTRL} \right) t \right]$$

Equation (2.5) indicates sidebands at $\pm n \omega_{ref}$ from the carrier, where ω_{ref} is the phase comparison frequency. Typical approaches to reducing the problem are using large capacitors in the loop filter (to keep ΔV to a minimum), and minimizing K_{VCO} to minimize the modulation index. However, both remedies have their downsides as well: increasing the loop filter capacitance requires increasing the chargepump current proportionally; K_{VCO} cannot be lowered indefinitely, because the tuning range still needs to cover the desired frequencies plus process, temperature and supply voltage variations.

2.3.Settling time

In modern telecommunications systems, the synthesizer often has strict requirements for settling time, defined as the time it takes for the synthesizer to settle to a given accuracy after a frequency step. In time division multiple access (TDMA) systems, the settling time specification is mostly due to the desire to use the same synthesizer for both transmit and receive modes, thus

saving power and area. In frequency hopping systems, the relatively frequent changing of the channel frequency is used to make sure that enough packets are received correctly even if a part of the frequency band would be blocked by strong interferers. Independent of the reason for changing the transmit or receive frequency, the system specifications usually set a limit on how fast this needs to be done, and this can be directly translated into a synthesizer settling time requirement[5].

In the phase-locked loop, being a low-pass control system by nature, the settling time is always inversely proportional to the loop bandwidth. Other constraints, such as stability, reference suppression, and close-in phase noise normally set the upper limit for the loop bandwidth. On the other hand, the settling time specification typically sets the fundamental lower limit.

Using the standard notation of feedback theory, a second-order loop has a closed-loop transfer function of

- Loop filter.
- Reference oscillator.

3.1.Single Chip

The single chip consists of a low noise, digital phase frequency detector (PFD), a precision charge pump, a programmable reference

- **Phase Frequency Detector (PFD) and Charge Pump:** The PFD takes inputs from the R counter and N counter ($N = BP + A$) and produces an output proportional to the phase and frequency difference between them. Figure 3.3 is a simplified schematic. The PFD includes a programmable delay element that
- **Prescaler($p/p+1$):** The dual-modulus prescaler ($P/P + 1$), along with the A counter and B counter, enables the large division ratio, N, to be realized ($N = BP + A$). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A counter and B counter. The prescaler is programmable. It can be set in soft-ware to 8/9, 16/17, 32/33, or 64/65. The A counter and B counter, in conjunction with the dual-modulus prescaler, make it possible to generate output

divider, programmable A counter and B counter, and a dual-modulus prescaler ($P/P + 1$).this chip is used for simplifying system architecture and reducing cost. In our system the single chip synthesizer is selected ADF4106 from Analog Device company because it has low phase noise, low spurious & low power consumption. The functional diagram of the single chip is shown in figure (3.2)[10]. The components of the single chip will illustrate as follows:

controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse.

frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is

$$f_{VCO} = [(P \times B) + A] \times \frac{f_{REFIN}}{R}$$

Eq(3.1)

Where :

f_{VCO} is the output frequency of the external voltage controlled oscillator (VCO).

P is the preset modulus of the dual-modulus prescaler (8/9, 16/17, etc.).

B is the preset divide ratio of the binary 13-bit counter (3 to 8191).

A is the preset divide ratio of the binary 6-bit swallow counter (0 to 63).

f_{REFIN} is the external reference frequency oscillator.

For our system the prescaler is programmed to 16/17.

- **R – counter:** The 14-bit R (reference) counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

3.2.Voltage controlled oscillator

The VCO must be cover the range (1.5-2.75) GHz with lower phase noise. Therefore we select RQRE -1500-27500 from ralton company to satisfy these requirements. It has the following specification:

- Tuning voltage ,DC :(1-20)volt.
- Typical o/p power : 7 dBm.
- D.C. power supply VCC: 10 volt with tolerance ± 0.25 .

3.3.Reference oscillator

The reference oscillator has a frequency 10 MHz & the reference counter (R-counter)in the single chip synthesizer must be set to 100 to obtain on 100KHz step size.

3.4.loop filter design

The loop filter is a passive 2nd order filter which is selected in the system because it has the following properties:

- the least complex loop filter.
- Smallest resistor thermal noise.

- Largest capacitor next to VCO to minimize the impact of VCO input capacitance.
- Maximum resistance to variation of VCO gain & PFD gain

The loop filter impedance is defined as the voltage output at VCO to the current injected at the charge pump in the single chip synthesizer. The expression of loop filter impedance $Z(s)$ & the corresponding poles & zeros are shown below at various filter orders is shown below[1]:

$$Z(s) = (1 + sT_2) / (A_0(1+sT_1)(1+sT_3)(1+sT_4))$$

Eq(3.2)

Where A_0 is filter coefficient & equal to $(c_1 + c_2)$ for passive loop filter

For passive 2nd order loop filter, the input impedance:

$$Z(s) = (1 + sC_2 R_1) / (s(C_1 + C_2)(1 + (sC_1C_2R_1) / (C_1 + C_2)))$$

Eq(3.3)

From the above equations , it should be clear :

$$T_2 = R_1C_2 \quad , \quad T_1 = R_1 C_1 C_2/A_0 \quad \& \quad A_0 = C_1 + C_2.$$

$$\text{Then } C_1 = A_0 T_1/T_2 \quad , \quad C_2 = A_0 - C_1 \quad , \quad R_1 = T_2/C_2.$$

$$T_2 = \zeta / (\omega_c^2 T_1)$$

Where ζ = optimization factor = 1.005 , $\omega_c = 2 \pi F_c$, F_c = loop B.W.,

$$T_1 = \{ [(1 + \zeta)^2 \tan^2 \phi + 4 \zeta]^{1/2} - (1 + \zeta) \tan \phi \} / (2 \omega_c) \quad , \quad \phi = \text{phase margin}$$

&

$$A_0 = \{ (K\phi K_{VCO}) / (N\omega_c^2) \} / \{ [(1 + \omega_c^2 T_2^2) / (1 + \omega_c^2 T_1^2)]^{1/2} \}$$

for the system : $C_1 = 12.2 \text{ nF}$, $R_1 = 5.46 \text{ K}\Omega$, & $C_2 = 12.8 \text{ nF}$

4.Results

A system is simulated by ADIPLLsim version 2.7 software & we obtain the following results: -

4.1. Phase noise

The phase noise of PLL frequency synthesizer & VCO is shown in the following table:

Offset frequency (Hz)	PLLfrequency synthesizer	VCO
100	-92.85	-171.3
1K	-92.4	-151.3
10 K	-92.74	-131.3
100 K	-90.19	-114.8
1 M	-117.0	-132.5

The c/c of phase noise with frequency for the system at output frequency 2.03 GHz is shown in figure 4.1

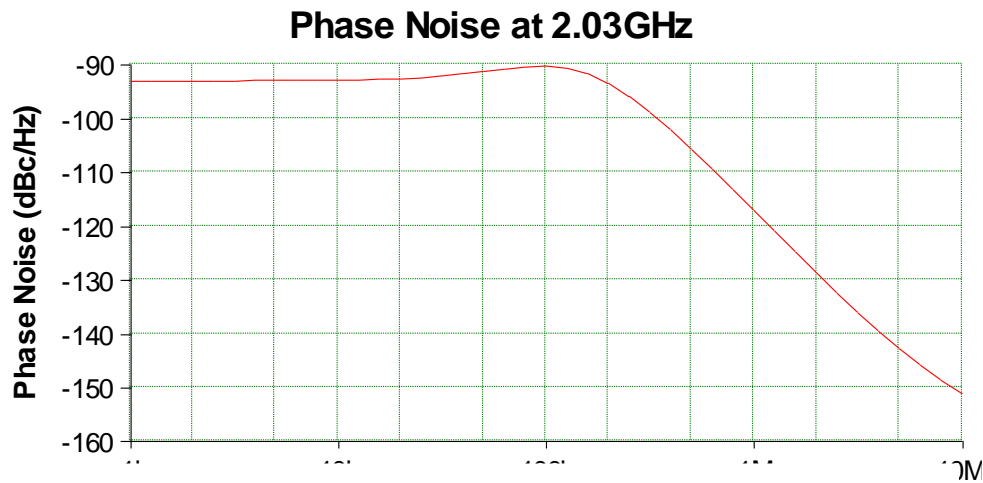


Figure 4.1. The c/c of phase noise with frequency for the system

The VCO c/c is simulated By ADIsimPLL software is shown in figure 4.2.

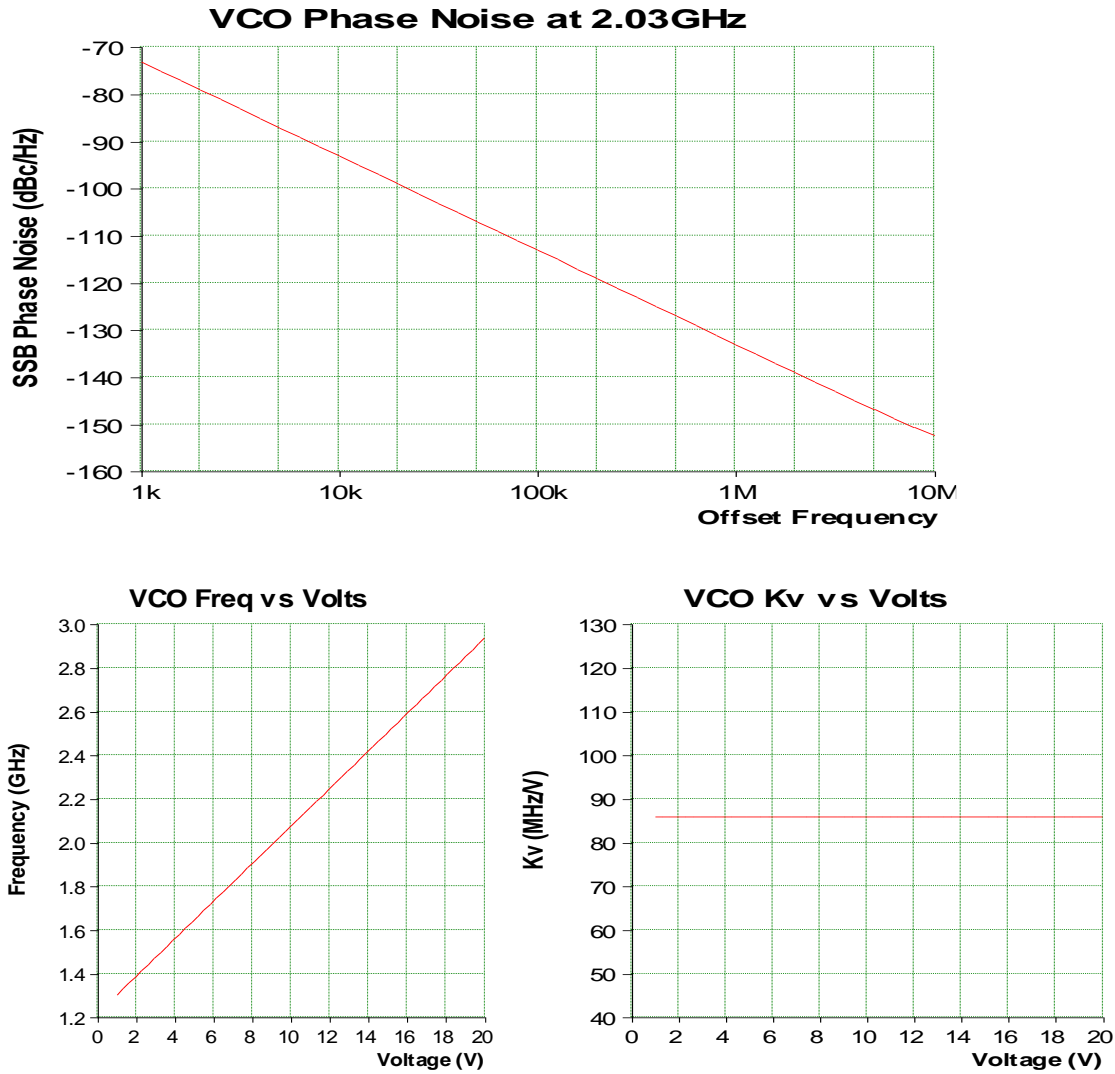


Figure 4.2. The c/c of VCO phase noise with frequency, VCO freq. with voltage & VCO Kv with voltage respectively

4.2.Reference Spurious

Noise and Jitter Calculations include the first 10 ref spurs

First three spurs: -100 dBc -100 dBc -100 dBc

4.3.switching speed

the switching speed for Frequency change from 1.5GHz to 2.75GHz is 36.4 μ s

The transient response for system from 1.5GHz to 1.65 GHz is shown in figure 4.3:

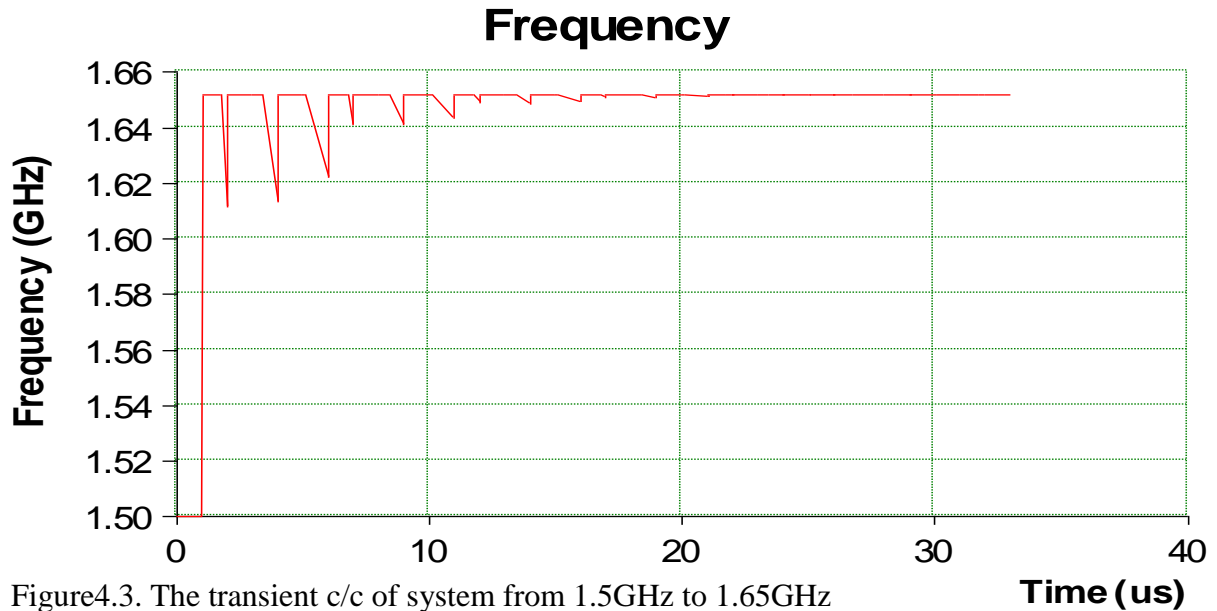


Figure4.3. The transient c/c of system from 1.5GHz to 1.65GHz

5. Discussion

The operation of implemented synthesizer was verified and various performance parameters have been checked & it is found they are within the system requirements. The first parameter is the phase noise, table 4-1 shows the highest phase noise in the system is -92.74dBc/Hz at 10KHz offset & The overshoot for phase noise @ offset frequency 100KHz as shown in figure 4.1 results from that the loop B.W. for PLL is 100KHz . The second parameter is the switching time is shown in figure 4.3 is $36.4\ \mu\text{s}$ is something close to theoretical value (4msec) in section 3.2.2 & the overshoots in figure 4.3 results from the transient case of frequency change & this transient case must be very small in time. The third parameter is a reference spurious, is illustrated from the results is -100dBc & this value satisfy the system requirements for spurious.

6. Conclusions

A frequency synthesizer with frequency range ($1.5 - 2.75$) GHz using single loop frequency synthesizer was design & implement. The development in I.C. technology provide the simplicity in the design of frequency synthesizer because it implements the PFD, prescaler & reference divider in single chip. this single chip has the following properties:

- Low power consumption.
- Small size, light weight.
- flexibility in selecting crystal oscillator frequencies to fit into the system frequency planning.
- High reliability.

From the results of this research, we conclude that the switching speed can be increase by increase loop bandwidth this results in increasing the reference frequency but it causes in increasing the step size. There are many techniques to implement this system.

We would present these techniques with their disadvantages.

There is Direct digital synthesis (DDS) can be used to implement this system but it has drawbacks , its main disadvantage include the fundamentals limit of B.W. (maximum frequency o/p is less than one half the clock rate). Expanded B.W. requires higher clock rates , & therefore faster logic and more critical manufacturing & testing processes. There is Hybrid technique (DDS as reference oscillator) can be used to implement this system successfully but it has high cost relative to implemented system. Multi Loop PLL can satisfy this frequency range but these loops with their mixers increase spurious o/p signals

, power dissipation , cost , size & complexity.

The major benefits of implemented system over the multi loop frequency synthesizer will illustrate in a fair comparison with previous work in 2003 includes design of an integrated CMOS PLL frequency synthesizer consists of two loops.

System parameters	Frequency range(GHz)	Step size	Switching time	Phase noise	Spurious level	Number of loops
Multi loop implemented In 2003	2.4 – 2.5	1MHz	30 μ s	-83 dB/Hz @ 10 KHz	-60 dBc	2
System implemented.	1.5 – 2.75	1MHz	36.4 μ s	-92dB/Hz @ 10 KHz	-100dBc	1

7. References

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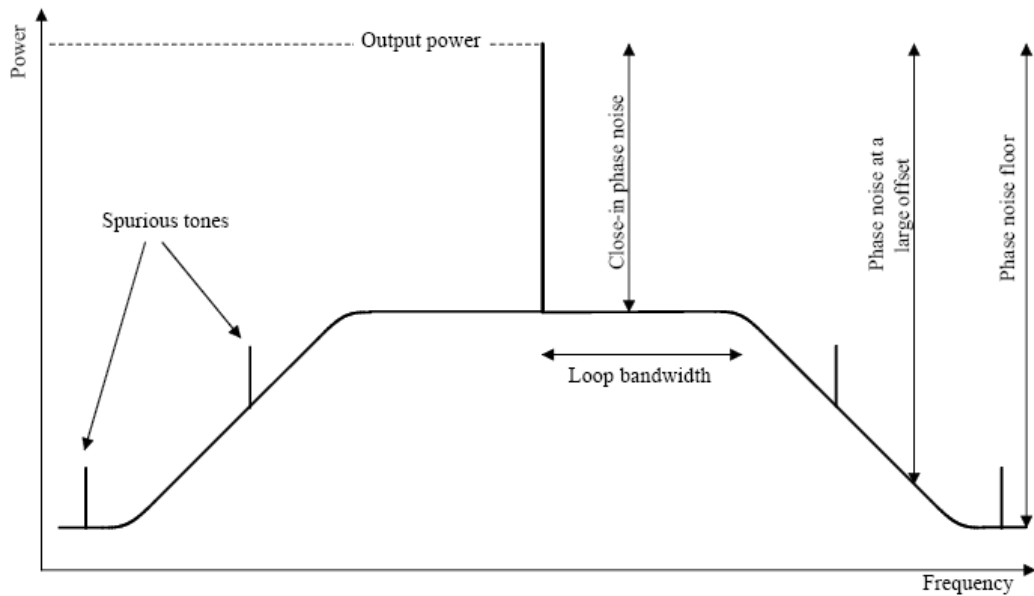


Figure 2.1. Non ideal components in the output spectrum of a PLL frequency synthesizer.

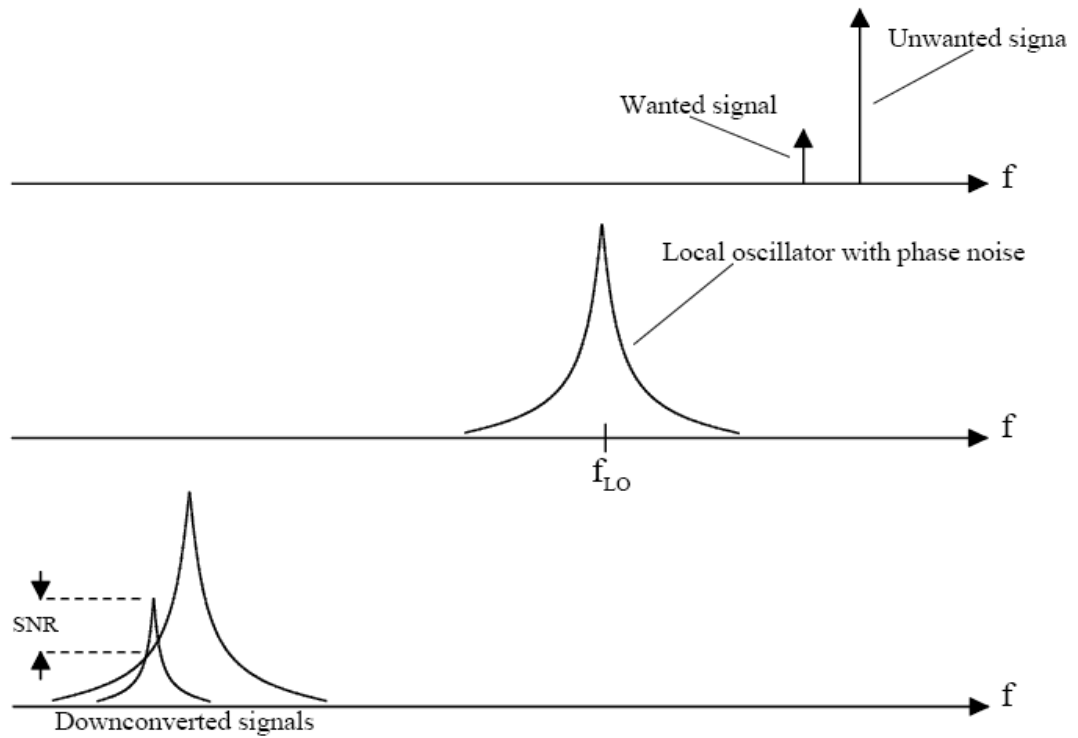


Figure 2.2. Reciprocal mixing

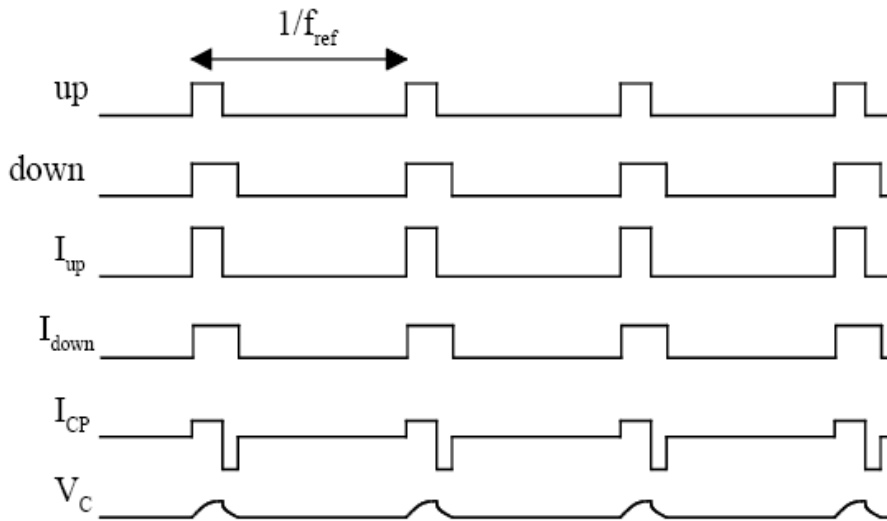


Figure 2.3 periodic signal generated by the charge pump.

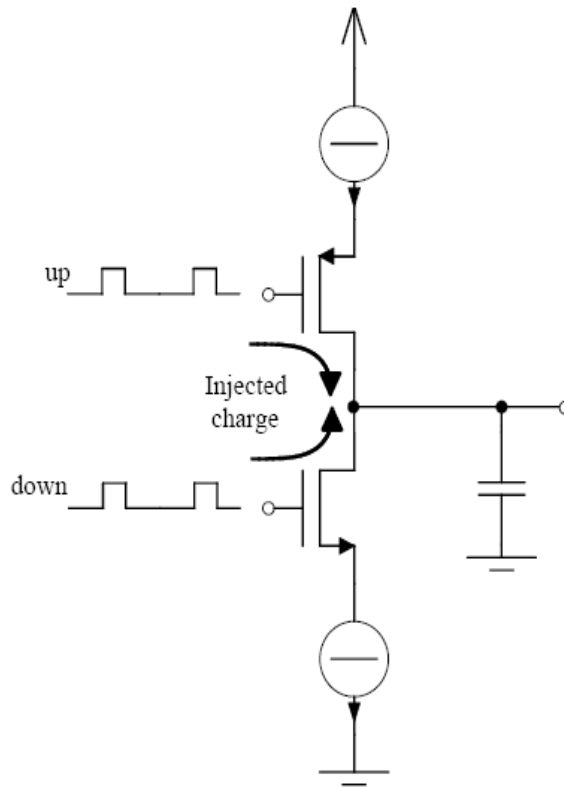
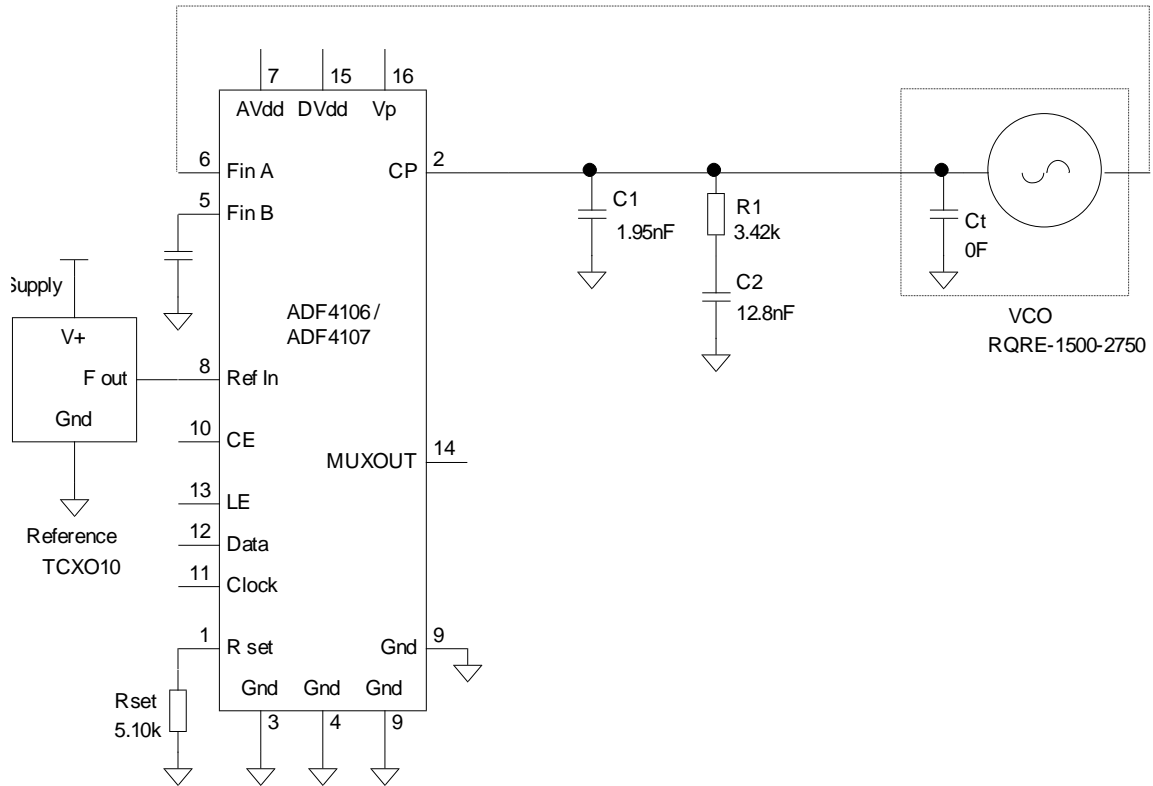


Figure 2.4 Charge injection in the chargepump switches.



- Notes ADF4106:
1. Vp is the Charge Pump power supply
 2. Vp >= Vdd
 3. CE must be HIGH to operate
 4. TSSOP pinouts shown
 5. Consult manufacturer's data sheet for full details

Figure 3.1. Schematic diagram of system

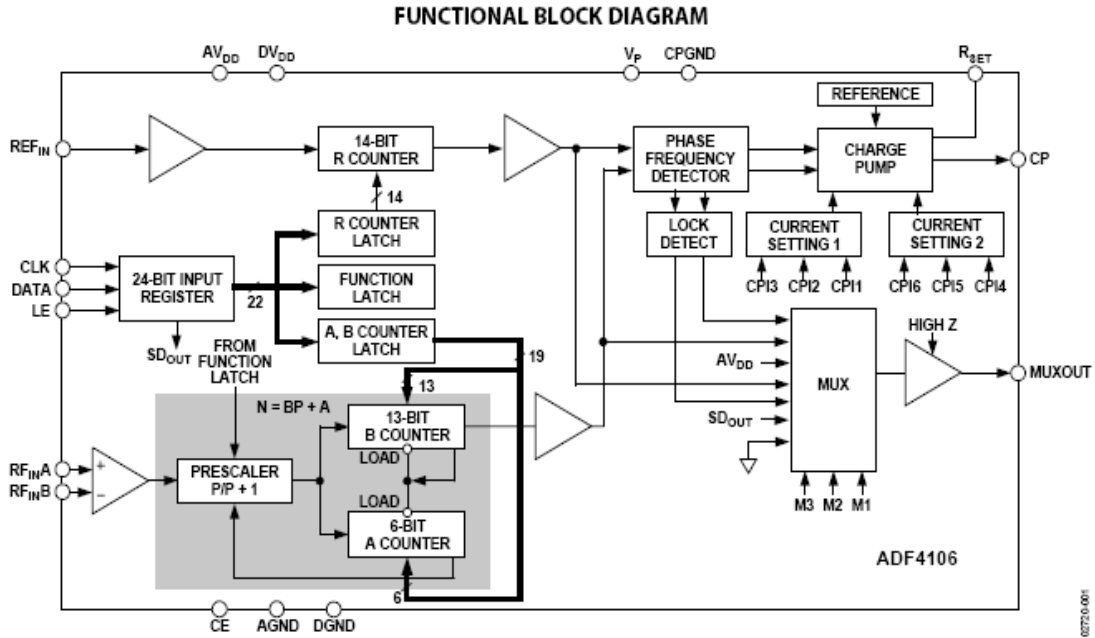


Figure 3.2. Functional diagram of single chip

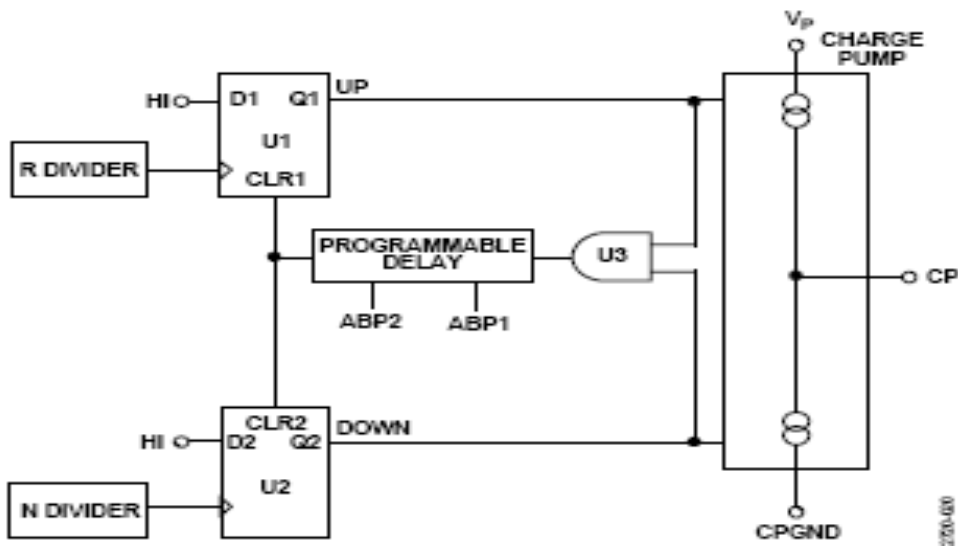


Figure 3.3. Schematic diagram of PFD & charge pump

تصميم وبناء مركب ترددات ذو سرعة تحويل عالية وضوضاء طوري قليل

علي محمد نوري

قسم هندسة المعلومات والاتصالات
كلية هندسة الخوارزمي / جامعة بغداد

الخلاصة:

يصف هذا البحث تصميم وبناء مركب ترددات باستخدام طريقة اقفال الطور احادي الدورة وبالمواصفات التالية :
مدى الترددات الخارجة (١٥٠٠-٢٧٥٠) ميكا هرتز، واقل سعة قفزة ١ ميكا هرتز، زمن تحويل ٣٦ مايكرو ثانية ومستوى ضوضاء طوري (-92) ديسيبل عند ١٠٠٠٠ هرتز من التردد الخارج. ومستوى الطفيليات - ١٠٠ ديسيبل

التطور الحاصل في الدوائر المتكاملة جهاز البساطة في تصميم مركب الترددات وذلك لأنه دمج كاشف التردد والطور، ومقسم التردد الثنائي، ومقسم التردد في شريحة رقيقة واحدة. لذلك منظومتنا تتكون من شريحة تحتوي على كل من (كاشف ترددات وطور ذو ضوضاء طوري قليل، مضخة شحنة دقيقة، مقسم ترددات مبرمج، ومقسم تردد ثنائي $(p/(p+1))$ مبرمج) مرشح ترددات واطنة، مذبذب ترددات ذو سيطرة جهدية، ومذبذب مرجعي. هذه الشريحة الرقيقة التي تحتوي كل من كاشف ترددات وطور مقسم ترددات مبرمج ومقسم تردد ثنائي تم استخدامها وذلك لأنها تمتلك المواصفات التالية:

قلة في استهلاك القدرة

حجم صغير ووزن خفيف

مرونة في اختيار تردد مذبذب البلورة بحيث يناسب خريطة التردد للمنظومة

وثوقية عالية

التطبيقات لهذا المركب في منظومات القفز بالتردد، واتصالات الأقمار الاصطناعية، والرادار

وذلك لأنها تمتلك خاصية ضوضاء طوري قليل وسرعة تحويل عالية ومستوى طفيليات اقل.